

L Number	Hits	Search Text	DB	Time stamp
1	33	(synthesiz\$3 synthesis) same (false near6 path)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/24 19:48
-	4131	(714/724,726,727,729).ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/23 12:15
-	644	((714/724,726,727,729).ccls.) and (boundary near2 scan)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/23 12:24
-	11	((714/724,726,727,729).ccls.) and (boundary near2 scan)) and delay near4 chain	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/23 12:24
-	21	((714/724,726,727,729).ccls.) and (boundary near2 scan)) and (delay near4 (chain measurement))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/23 12:36
-	366	((714/724,726,727,729).ccls.) and (boundary near2 scan near4 (cell device buffer))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/23 12:35
-	12	((714/724,726,727,729).ccls.) and (boundary near2 scan near4 (cell device buffer))) and (delay near4 (chain measurement))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/23 12:33
-	0	((714/724,726,727,729).ccls.) and (boundary near2 scan near4 (cell device buffer))) and (delay near4 (chain measurement))) not (((714/724,726,727,729).ccls.) and (boundary near2 scan)) and (delay near4 (chain measurement)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/23 12:26
-	9	((714/724,726,727,729).ccls.) and (boundary near2 scan)) and (delay near4 (chain measurement))) not (((714/724,726,727,729).ccls.) and (boundary near2 scan near4 (cell device buffer))) and (delay near4 (chain measurement)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/23 12:27
-	286	((714/724,726,727,729).ccls.) and (boundary near2 scan near4 (cell device buffer))) and (bypass multiplex\$2 MUX)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/23 12:33
-	109	((714/724,726,727,729).ccls.) and ((boundary near2 scan near4 (cell device buffer)) same (bypass multiplex\$2 mux))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/23 12:35
-	177	((714/724,726,727,729).ccls.) and ((boundary near2 scan near4 (cell device buffer)) same (bypass multiplex\$2 mux))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/23 13:36
-	7	((714/724,726,727,729).ccls.) and ((boundary near2 scan near4 (cell device buffer)) same (bypass multiplex\$2 mux))) and (delay near4 (chain measurement))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/23 13:37

-	12	((714/724,726,727,729).ccls.) and ((boundary near2 scan near4 (cell device buffer)) same (bypass multiplex\$2 mux)) and (delay near4 (chain measur\$5))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/24 15:01
-	5	((714/724,726,727,729).ccls.) and ((boundary near2 scan near4 (cell device buffer)) same (bypass multiplex\$2 mux)) and (delay near4 (chain measur\$5))) not (((714/724,726,727,729).ccls.) and ((boundary near2 scan near4 (cell device buffer)) same (bypass multiplex\$2 mux)) and (delay near4 (chain measurement)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/23 13:18
-	0	5710779.pn	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/23 13:19
-	2	US-5710779\$.did.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/23 14:11
-	1		USPAT; US-PGPUB	2004/07/23 13:21
-	1		USPAT; US-PGPUB	2004/07/23 13:22
-	1		USPAT; US-PGPUB	2004/07/23 13:22
-	1		USPAT; US-PGPUB	2004/07/23 13:23
-	1		USPAT; US-PGPUB	2004/07/23 13:24
-	1		USPAT; US-PGPUB	2004/07/23 13:24
-	1		USPAT; US-PGPUB	2004/07/23 13:27
-	304	((714/724,726,727,729).ccls.) and ((scan near4 (cell device buffer)) same (bypass multiplex\$2 mux))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/24 15:00
-	17	((714/724,726,727,729).ccls.) and ((scan near4 (cell device buffer)) same (bypass multiplex\$2 mux)) and (delay near4 (chain measurement))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/23 13:48
-	202	((714/724,726,727,729).ccls.) and ((scan near4 (cell device buffer)) same (bypass multiplex\$2 mux)) and (TAP JTAG "1149" "test access port")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/23 13:48
-	32	((714/724,726,727,729).ccls.) and ((scan near4 (cell device buffer)) same (bypass multiplex\$2 mux)) and (TAP JTAG "1149" "test access port")) and (delay near4 (test chain measurement))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/23 13:49
-	1	\$-0994361\$.did.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/23 14:12
-	59	(boundary near2 scan) same (delay near4 (test\$3 fault))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/24 15:02

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE



Membership Publications/Services Standards Conferences Careers/Jobs

**IEEE Xplore<sup>®</sup>**  
 RELEASE 1.8

 Welcome  
 United States Patent and Trademark Office


» Se.

[Help](#) [FAQ](#) [Terms](#) [IEEE Peer Review](#)
[Quick Links](#)
Welcome to IEEE Xplore<sup>®</sup>

- ☐ Home
- ☐ What Can I Access?
- ☐ Log-out

Tables of Contents

- ☐ Journals & Magazines
- ☐ Conference Proceedings
- ☐ Standards

Search

- ☐ By Author
- ☐ Basic
- ☐ Advanced

Member Services

- ☐ Join IEEE
- ☐ Establish IEEE Web Account
- ☐ Access the IEEE Member Digital Library

IEEE Enterprise

- ☐ Access the IEEE Enterprise File Cabinet

Print Format

Your search matched **80** of **1053485** documents.A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.**Refine This Search:**

You may refine your search by editing the current search expression or enter a new one in the text box.

(boundary &lt;near/2&gt; scan) &lt;and&gt; delay &lt;near/6&gt; (te

☐ Check to search within this result set**Results Key:****JNL** = Journal or Magazine **CNF** = Conference **STD** = Standard**1 Automated synthesis of phase shifters for built-in self-test applicati***Rajski, J.; Tamarapalli, N.; Tyszer, J.;*

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction on , Volume: 19 , Issue: 10 , Oct. 2000

Pages:1175 - 1188

[\[Abstract\]](#) [\[PDF Full-Text \(320 KB\)\]](#) **IEEE JNL**
**2 Synthesis for parallel scan: applications to partial scan and robust p delay fault testability***Bhatia, S.; Jha, N.J.;*

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction on , Volume: 15 , Issue: 2 , Feb. 1996

Pages:228 - 243

[\[Abstract\]](#) [\[PDF Full-Text \(1712 KB\)\]](#) **IEEE JNL**
**3 Scan-based transition test***Savir, J.; Patil, S.;*

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction on , Volume: 12 , Issue: 8 , Aug. 1993

Pages:1232 - 1241

[\[Abstract\]](#) [\[PDF Full-Text \(860 KB\)\]](#) **IEEE JNL**
**4 Delay-fault test generation and synthesis for testability under a sta scan design methodology***Cheng, K.-T.; Devadas, S.; Keutzer, K.;*

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction on , Volume: 12 , Issue: 8 , Aug. 1993

Pages:1217 - 1231

[\[Abstract\]](#) [\[PDF Full-Text \(1368 KB\)\]](#) IEEE JNL

---

**5 Simulator for path-delay faults on mixed-level circuits**

*Yim, Y.T.; Kang, Y.S.; Kang, S.;*

Circuits, Devices and Systems, IEE Proceedings [see also IEE Proceedings G-Circuits, Devices and Systems] , Volume: 144 , Issue: 4 , Aug. 1997

Pages:236 - 242

[\[Abstract\]](#) [\[PDF Full-Text \(636 KB\)\]](#) IEEE JNL

---

**6 A new IEEE 1149.1 boundary scan design for the detection of delay defects**

*Sungju Park; Taehyung Kim;*

Design, Automation and Test in Europe Conference and Exhibition 2000. Proceedings , 27-30 March 2000

Pages:458 - 462

[\[Abstract\]](#) [\[PDF Full-Text \(56 KB\)\]](#) IEEE CNF

---

**7 Peak-power reduction for multiple-scan circuits during test application**

*Kuen-Jong Lee; Tsung-Chu Haung; Jih-Jeen Chen;*

Test Symposium, 2000. (ATS 2000). Proceedings of the Ninth Asian , 4-6 Dec 2000

Pages:453 - 458

[\[Abstract\]](#) [\[PDF Full-Text \(520 KB\)\]](#) IEEE CNF

---

**8 On testing the path delay faults of a microprocessor using its instruction set**

*Wei-Cheng Lai; Krstic, A.; Kwang-Ting Cheng;*

VLSI Test Symposium, 2000. Proceedings. 18th IEEE , 30 April-4 May 2000

Pages:15 - 20

[\[Abstract\]](#) [\[PDF Full-Text \(56 KB\)\]](#) IEEE CNF

---

**9 At-speed testing of delay faults for Motorola's MPC7400, a PowerPC microprocessor**

*Tendolkar, N.; Molyneaux, R.; Pyron, C.; Raina, R.;*

VLSI Test Symposium, 2000. Proceedings. 18th IEEE , 30 April-4 May 2000

Pages:3 - 8

[\[Abstract\]](#) [\[PDF Full-Text \(76 KB\)\]](#) IEEE CNF

---

**10 Proceedings 18th IEEE VLSI Test Symposium**

VLSI Test Symposium, 2000. Proceedings. 18th IEEE , 30 April-4 May 2000

[\[Abstract\]](#) [\[PDF Full-Text \(728 KB\)\]](#) IEEE CNF

---

**11 Critical hazard free test generation for asynchronous circuits**

*Khoche, A.; Brunvand, E.;*

VLSI Test Symposium, 1997., 15th IEEE , 27 April-1 May 1997

Pages:203 - 208

[\[Abstract\]](#) [\[PDF Full-Text \(496 KB\)\]](#) IEEE CNF

---

**12 Proceedings. 15th IEEE VLSI Test Symposium (Cat. No.97TB10012)**

VLSI Test Symposium, 1997., 15th IEEE , 27 April-1 May 1997

[\[Abstract\]](#) [\[PDF Full-Text \(1892 KB\)\]](#) IEEE CNF

---

**13 Design for testability: today and in the future**

*Williams, T.W.;*

VLSI Design, 1997. Proceedings., Tenth International Conference on , 4-7 Jan 1997

Pages:314 - 315

[\[Abstract\]](#) [\[PDF Full-Text \(156 KB\)\]](#) IEEE CNF

---

**14 Early capture for boundary scan timing measurements**

*Lofstrom, K.;*

Test Conference, 1996. Proceedings., International , 20-25 Oct. 1996

Pages:417 - 422

[\[Abstract\]](#) [\[PDF Full-Text \(560 KB\)\]](#) IEEE CNF

---

**15 Hybrid pin control using boundary-scan and its applications**

*Ke, W.;*

Test Symposium, 1996., Proceedings of the Fifth Asian , 20-22 Nov. 1996

Pages:44 - 49

[\[Abstract\]](#) [\[PDF Full-Text \(408 KB\)\]](#) IEEE CNF

---

[1](#) [2](#) [3](#) [4](#) [5](#) [6](#) [Next](#)

---

[Home](#) | [Log-out](#) | [Journals](#) | [Conference Proceedings](#) | [Standards](#) | [Search by Author](#) | [Basic Search](#) | [Advanced Search](#) | [Join IEEE](#) | [Web Account](#) | [New this week](#) | [OPAC Linking Information](#) | [Your Feedback](#) | [Technical Support](#) | [Email Alerting](#) | [No Robots Please](#) | [Release Notes](#) | [IEEE Online Publications](#) | [Help](#) | [FAQ](#) | [Terms](#) | [Back to Top](#)

Copyright © 2004 IEEE — All rights reserved